UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,739	10/30/2003	Binh Vo	015114-068400US	3284

26059 7590 02/09/2009

TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
NGUYEN, STEVE N	
ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
02/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,739	VO ET AL.	
	Examiner	Art Unit	
	STEVE NGUYEN	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *23 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-24 are currently pending.

Specification

In view of the Applicant's Remarks, the Examiner withdraws all objections to the specification.

Claim Rejections - 35 USC § 112

The U.S.C. 112, first paragraph rejection of claims 2, 23, and 24 has been withdrawn in view of the amended claims.

Election/Restrictions

Newly submitted claims 23 and 24 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claims 23 and 24 are directed to testing clock signal resources and is a separate embodiment from claim 1 that is not intended to be used together. For example, the embodiment of claim 1 is taught on page 5, paragraph 34 and in Fig. 2B. The embodiment of claims 23 and 24 is clearly a distinct embodiment from that of claim 1, as taught on page 6, paragraph 38 and Fig. 2C. It is clear from Fig. 2C that the fan-in

and fan-out resources required in claim 1, for example, are not present in the figure or methods of Figs. 2D and 2F.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 23 and 24 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

Claim 15 is directed to a “computer system” comprising a “statistical failure isolation tool” and an "adaptive failure isolation tool". The remaining limitations are functional language. It is noted that as per MPEP 2114, apparatus claims must be structurally distinguishable from the prior art. The manner of operating the device, as in the present claim, does not differentiate the apparatus from the prior art.

Response to Arguments

Applicant's arguments filed 12/01/2008 have been fully considered but they are not persuasive.

Applicant argues that since the identification of defective resources does not occur until the tests are done, Culbertson does not generate new test patterns. Accordingly, Culbertson does not teach or suggest "generating new test patterns

including program bits" that define new test paths for testing a first routing resource of the subset of the routing resources," as recited in claim 1.

The Examiner asserts that Culbertson identifies defective resources in intermediate stages of testing and not only at the end of the reconfiguration of resources as alleged by Applicant. For example, Culbertson teaches performing a test iteration (col. 8, lines 45-50) to identify a first subset of faulty resources as marked in Fig. 5C (elements 71-71d; col. 8, lines 50-57). The test method then generates new test patterns by reconfiguring the devices as shown in Fig. 5C to end up with the subset shown in Fig. 5D.

Applicant further argues that Culbertson does not teach "wherein each of the new test paths includes: the first routing resource" because not all of the new generators in Fig. 5C include the same resource. Applicant points out that generator 95 does not include resource 71b.

The Examiner notes that the Office Action stated any one of 71b, 71c, or 71d is “a first routing resource”. If resource 71d is a first resource, then test path 95 is one test path. The illustrations in Fig. 5 are grossly simplified in order to explain the operation of Culbertson. Any person skilled in the art would have recognized that an actual circuit would have been more complex than the one shown in Fig. 5 and that additional test paths including resource 71d would have been generated, such as those shown in Fig. 14.

The Applicant argues that whether something could be done is not the legal standard. The standard is whether one would be motivated to make a modification, with an explicit rationale for how and why the modification would be done.

The Examiner asserts that teaching, suggestion, or motivation (TSM) is not the only rationale that may be relied upon to support a conclusion of obviousness. Not finding TSM does not imply non-obviousness.

In this case, Culbertson already acknowledges that the resources could comprise fan-in and fan-out resources (col. 4, line 59). One or ordinary skill in the art would have recognized that the circuit of Culbertson would have had data inputted and outputted from it at some position in the circuit, and that fan-in and fan-out resources would have been a necessity. Furthermore, there are only a finite number of ways that the resources of Culbertson could have been arranged, and they would have all required fan-in and fan-out resources because each arrangement described by Culbertson receives and outputs data. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include combinations of fan-in and fan-out resources in the new test paths as a matter of ordinary ingenuity and common sense.

The Examiner disagrees with the Applicant and maintains all rejections of claims 1-22. All amendments and arguments by the Applicant have been considered. It is the Examiner's conclusion that claims 1-22 are not patentably distinct or non-obvious over the prior art of record. Therefore, the rejection is maintained below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3, 5-10, and 12-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Culbertson et al (US Pat. 5,790,771; hereinafter referred to as Culbertson).

As per claims 1 and 9:

Culbertson teaches a method for isolating failed routing resources on a programmable integrated circuit, the method comprising:

- receiving a plurality of failed test patterns, wherein a test pattern includes program bits that define how routing resources on the programmable integrated circuit are connected to form a test path (col. 6, lines 34-42), wherein a test pattern is designated as failing when a result from a test path is erroneous,

wherein the result of the failed test path is created by applying one or more test values to the failed test path (col. 6, lines 43-52);

- identifying a subset of the routing resources, wherein the subset comprises one or more routing resources that respectively occur in the most failed test paths (col. 6, line 65- col. 7, line 5); and
- generating new test patterns including program bits that define new test paths for testing a first routing resource of the subset of the routing resources (Fig. 4B; 59), wherein each of the new test paths includes:
- the first routing resource (Fig. 5C; any one of 71b, 71c, or 71d); and
- a combination, not included in the other new test paths, routing resources that are programmably connectable to the first routing resource (Fig. 14; col. 9, lines 11-14),

Not explicitly disclosed by Culbertson is the combination of routing resources programmably connectable to the first routing resource are fan-in and fan- out resources. However, Culbertson states that the routing resources shown in Fig. 1 could be fan-in and fan- out resources (col. 4, line 59). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include combinations of fan-in and fan- out resources in the new test paths. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have been motivated to do so since it is suggested by Culbertson.

Also not explicitly disclosed by Culbertson is wherein the new test paths test every combination of fan-in and fan-out resources that are programmably connectable to the first routing resource. However, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to test every combination of fan-in and fan-out resources that are programmably connectable to the first routing resource. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because the key to isolating a faulty resource is redundant testing in which each resource is tested multiple times, each time grouped with a different set of other resources (col. 6, lines 26-29).

As per claim 15:

Culbertson teaches a computer system for isolating failed routing resources on a programmable integrated circuit, the computer system comprising:

- a statistical failure isolation (SFI) tool, wherein the SFI tool:
- (a) receives a file (col. 5, lines 41-43) including a plurality of failed test patterns that generated erroneous results when test values were applied to a set of failed test paths (col. 6, lines 34-42), wherein a test pattern includes program bits that define how routing resources on the programmable integrated circuit are connected to form a test path (col. 6, lines 43-52);
- (b) determines routing resources along each failed test path (Fig. 5B);
- (d) identifies a subset of the routing resources, wherein the subset comprises one or more resources having the highest number of occurrences (col. 6, line 65-col. 7, line 5); and

- an adaptive failure isolation (AFI) tool that subsequent to completion of (b)-(d) generates new test patterns including program bits that define new test paths for testing the subset of the routing resources (Fig. 4B; 59).

Not explicitly disclosed by Culbertson is the SFI tool calculates a total number of occurrences of each resource in the failed test paths received in the file, at least one resource occurring in two failed test paths. However, Culbertson teaches identifying each resource in the failed test paths in a lookup table (col. 5, lines 48-54). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to calculate the total number of occurrences of each resource in the failed test paths. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that each of the resources would have been identified multiple times in the redundant testing (col. 6, lines 27-30); and that keeping a count was only a matter of design choice accounted for by Culbertson in col. 5, lines 65-67.

As per claim 2:

Culbertson further teaches the method according to claim 1 further comprising: testing the new test patterns using a test system to isolate routing resources among the subset of the routing resources that caused the erroneous results in the failed test patterns (Fig. 2).

As per claims 3, 13, 18:

Culbertson further teaches the wherein generating the new test patterns includes program bits that define new test paths for testing every routing resource of the subset;

wherein for each routing resource of the subset, the new test paths route through every combination of fan-in resources and fan-out resources that are programmably connectable to that routing resource of the subset (col. 6, lines 26-30, 67).

As per claim 5:

Culbertson further teaches the method according to claim 1 wherein each of the failed test paths and the new test paths connect a control point to an observation point on the programmable integrated circuit (col. 4, line 59).

As per claims 6, 14, 19:

Culbertson teaches the method above, but does not explicitly disclose wherein the routing resources have more than 1000 times as many routing resources as the subset of routing resources. However, one of ordinary skill in the art at the time the invention was made would have recognized that a modern circuit would have contained many thousands of routing resources.

As per claims 7, 10, 16:

Culbertson further teaches receiving a test log file that indicates the observation points for the failed test paths (Fig. 2; 32).

As per claims 8 and 20:

Culbertson teaches the method above. Not explicitly disclosed is wherein identifying the subset of the routing resources that occur most frequently in the failed test paths further comprises: extracting the routing resources that are connected along each of the failed test paths using a connectivity graph. However, it would have been

obvious to one of ordinary skill in the art to do so because Culbertson shows the extraction of failed paths using the drawing of Fig. 5.

As per claims 12 and 17:

Culbertson further teaches the computer program product of claim 9 further comprising: code for testing the new test patterns to isolate routing resources among the subset that caused the erroneous results in the failed test patterns (Fig. 4).

As per claim 21:

Culbertson further teaches the method of claim 1, wherein each of the new test paths is used to determine whether the resources of the subset have actually failed (col. 5, lines 38-39).

As per claim 22:

Culbertson further teaches the method of claim 1, wherein the erroneous result of a failed test path is an output value of the failed test path that does not equal an expected value (col. 6, lines 51-57).

Claims 4 and 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Culbertson in view of Abramovici et al (US Pat. 6,966,020; hereinafter referred to as Abramovici).

As per claims 4 and 11:

Culbertson teaches the method above. Not explicitly disclosed is wherein generating the new test patterns for the subset of the routing resources further comprises: generating new test patterns for test paths that route through clock and clear

signal routing resources. However, Abramovici teaches programmable logic of a boundary-scan interface (col. 5, lines 59-62).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to generate new test patterns for test paths that route through the clock and clear signal routing resources necessarily present in a boundary scan interface. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the routing resources of Culbertson could have been used in a boundary scan interface (Culbertson; col. 4, lines 56-60).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVE NGUYEN whose telephone number is (571)272-7214. The examiner can normally be reached on M-F, 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner, Art Unit 2117

Steve Nguyen
Examiner
Art Unit 2117